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Intellectual Property Administration
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PATENT APPLICATION

ATTORNEY DOCKET NO. 200304299-1

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s):	Sompong Paul Olarig et al.	Confirmation No.:	7506
Application No.:	10/039,010	Examiner:	Chery, Mardochee
Filing Date:	December 31, 2001	Group Art Unit:	2188

Title: Supporting Interleaved Read/Write Operations from/to Multiple Target Devices

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TRANSMITTAL OF REPLY BRIEF

Transmitted herewith is the Reply Brief with respect to the Examiner's Answer mailed on December 9, 2008 .

This Reply Brief is being filed pursuant to 37 CFR 1.193(b) within two months of the date of the Examiner's Answer.

(Note: Extensions of time are not allowed under 37 CFR 1.136(a))

(Note: Failure to file a Reply Brief will result in dismissal of the Appeal as to the claims made subject to an expressly stated new ground rejection.)

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Respectfully submitted,

Sompong Paul Olarig et al.

By

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Date : February 9, 2009

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For:	Supporting Interleaved Read/Write Operations from/to Multiple Target Devices	Atty. Docket:	NUHP:0107/FLE/DOO 200304299-1

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February 9, 2009 — Katey P. Hines
Date

REPLY BRIEF PURSUANT TO 37 C.F.R. § 41.41

This Reply Brief is being filed pursuant to 37 C.F.R. §41.41 and in response to the Examiner's Answer mailed on December 9, 2008. Specifically, this Reply Brief addresses the Examiner's misapplication of Leung et al., U.S. Patent No. 6,272,577 (hereinafter referred to as "the Leung reference"), Guttag et al., U.S. Patent No. 6,272,577 (hereinafter referred to as "the Leung reference"), Gupta et al., U.S. Patent No. 6,405,286 (hereinafter referred to as "the Gupta reference"), and Blaner, U.S. Patent No. 5,737,575 (hereinafter referred to as "the Blaner reference"). By the present Reply, Appellants stress previously made arguments and provide additional arguments regarding assertions by the Examiner in the Examiner's Answer. In addition to the present remarks, Appellants respectfully request that the Board consider Appellants' complete arguments set forth in the Appeal Brief filed September 22, 2008.

A. **Examiner's Argument Regarding Claim 1:**

In attempting to teach the recitation of independent claim 1 directed to the *same* single base address being associating with *each* of the plurality of target devices, the Examiner, in the Examiner's Answer, argued that the Guttag reference discloses a one to one correspondence between the "plurality of memories" and the "corresponding fixed base address." *See* Examiner's Answer, pages 5 and 23. In fact, the Guttag reference does not describe the *same* single base address being associating with *each* of the plurality of target devices. At best, the Guttag reference describes a plurality of memories that, at best, correspond to *both* a parameter memory base address *and* a data memory base address, that is, *two* base addresses. *See* Guttag, col. 5, lines 63-66. Thus, because the Guttag reference describes utilization of a *plurality* of base addresses that correspond to a plurality of memories, the Guttag reference cannot be read as describing the *same* single base address being associating with *each* of the plurality of target devices, as recited in independent claim 1.

Furthermore, the Examiner argued that the Leung reference also discloses associating the pluarility of target devices with a single base memory address, citing col. 3, lines 31-34 of the Leung reference. *See* Examiner's Answer, page 23. This cited portion of the Leung reference specifically describes memory modules as equipped with independent address and command decoders so that they function as independent units, *each with their own base address*. *See* Leung, col. 3, lines 31-34. Since the Leung reference specifically describes the memory modules as each having their *own* base address, the Examiner is simply incorrect in the assertion that that Leung discloses associating the pluarility of target devices with a *single* base memory address.

Accordingly, the Examiner has failed to show that the Leung reference and/or the Guttag references, taken either alone or in hypothetical combination, teach all elements of independent claim 1. Accordingly, Appellants respectfully request the Board reverse the Examiner's rejection under 35 U.S.C. § 103 of independent claim 1, as well as all claims depending therefrom.

B. **Examiner's Argument Regarding Claims 5 and 6:**

In the Examiner's Answer, the Examiner argued that the recitations "the target devices comprise input/output controllers" and "the target devices comprise disk array controllers" in claims 5 and 6 are taught by the Leung reference because the term "comprise" is not equivalent to the term "are", and thus, the recitations of "input/output controllers" and "disk array controllers" need not be described in the cited art. *See* Examiner's Answer, page 27. The Examiner is directed to review M.P.E.P. 2111.03 that details the usage of transitional phrases, such as, comprise, to define the scope of the claim. In short, M.P.E.P. 2111.03 states that the term "comprise" specifically *includes* the element recited, but does not exclude *other* elements from the claim. Thus, while the Examiner is free to show that the prior art includes additional elements, the Examiner must show that the prior art teachings *include* input/output controllers and disk array controllers to properly maintain a Section 103 rejection of claims 5 and 6. The Leung reference, at best, shows memory arrays that may be simultaneously written to, but does not show that these memory arrays comprise either input/output controllers and/or disk array controllers as recited in claim 5 and 6.

Furthermore, the Examiner argued that the recited target devices of independent claim 1 and of dependent claims 5 and 6 may be different target devices. *See* Examiner's Answer, page 27. The Examiner is reminded that the term "the target devices" in claims 5 and 6 must necessarily be the same target devices as referenced in independent claim 1 because of the use of the article "the" in claims 5 and 6. That is, "the target devices" of claims 5 and 6 refer to target devices of claim 1 for antecedent basis. Thus, target devices in independent claim 1 may not be read as a plurality of memory arrays in the Leung reference, while the target devices of claims 5 and 6 are read as an I/O module in the Leung reference. Accordingly, because the Examiner has construed target devices as a plurality of memory arrays in the rejection of claim 1, and because the plurality of memory arrays of the Leung reference do not include either input/output controllers and/or disk array controllers, the Leung reference fails to teach all elements of claims 5 and 6. Accordingly, because the Examiner has failed to show all elements of claims 5 and 6 in the prior art, Appellants respectfully request the Board reverse the Examiner's rejection under 35 U.S.C. § 103 of claims 5 and 6.

C. **Examiner's Argument Regarding Claim 9:**

In the Examiner's Answer, with respect to independent claim 9, the Examiner argued that the Guttag reference discloses a plurality of n processors with a corresponding plurality of memories, with the plurality of memories having a corresponding base address. *See* Examiner's Answer, page 29. As described above with respect to the rejection of independent claim 1, the Guttag reference describes a plurality of memories that, at best, correspond to *both* a parameter memory base address *and* a data memory base address, that is, *two* base addresses. *See* Guttag, col. 5, lines 63-66. Accordingly, the Guttag reference cannot be read as describing accessing

first and second portions of memory with a *single base address* associated with both the first target device and the second target device, as recited in independent claim 9.

The Leung reference also cannot be read as describing accessing first and second portions of memory with a single base address associated with both the first target device and the second target device, as recited in independent claim 9 because the Leung reference specifically describes its memory modules as equipped with independent address and command decoders so that they function as independent units, *each with their own base address*. *See* Leung, col. 3, lines 31-34.

Furthermore, neither the Leung reference nor the Guttag reference describe accessing the first and second portions of memory with a single base address associated with both the *first target device* and the *second target device*, wherein the *first and the second target devices* are associated with the same single base address. Specifically, the Leung and Guttag references describe only the access of memory; they do not describe association of a first and a second target device, *separate from memory*, associated with the same single base address, as recited in independent claim 9. Accordingly, the Leung and Guttag references cannot be read as teaching accessing the first and second portions of memory with a *single base address* associated with *both* the first target device and the second target device, wherein the first and the second target devices are associated with the *same single base address*.

As such, the Examiner has failed to show that the Leung reference and/or the Guttag reference, taken either alone or in hypothetical combination, teach all elements of independent

claim 9. Therefore, Appellants respectfully request the Board reverse the Examiner's rejection under 35 U.S.C. § 103 of independent claim 9, as well as all claims depending therefrom.

D. **Examiner's Argument Regarding Claims 10 and 11:**

Similar to claims 5 and 6 discussed above, claims 10 and 11 recite "the target devices comprise input/output controllers" and "the target devices comprise disk array controllers," to which the Examiner argued the non-limiting nature of the term "comprise." *See* Examiner's Answer, page 30. As set forth above with respect to the rejection of claims 5 and 6, the Examiner must show that the prior art teachings *include* input/output controllers and disk array controllers to properly maintain a Section 103 rejection of claims 10 and 11. *See* M.P.E.P. 2111.03. The Leung reference, at best shows memory arrays that may be simultaneously written to, but does not show that these memory arrays comprise either input/output controllers and/or disk array controllers as recited in claim 10 and 11. Therefore, the applied prior art fails to teach all elements of claims 10 and 11. Accordingly, because the Examiner has failed to show all elements of claims 10 and 11 in the prior art, Appellants respectfully request the Board reverse the Examiner's rejection under 35 U.S.C. § 103 of claims 10 and 11.

E. **Examiner's Argument Regarding Claims 16 and 25:**

In the Examiner's Answer, with respect to independent claims 16 and 25, the Examiner argued that the rationale with respect to the rejection of independent claim 1 could be applied to the rejection of independent claims 16 and 25. *See* Examiner's Answer, page 32. As described above with respect to the rejection of independent claim 1, the Guttag reference describes a plurality of memories that, at best, correspond to *both* a parameter memory base address *and* a

data memory base address, that is, *two* base addresses. *See* Guttag, col. 5, lines 63-66. Accordingly, the Guttag reference cannot be read as describing an initiator device is configured to multicast the transaction request to the plurality of target devices using a *single base address* associated with the plurality of target devices, wherein the same *single base address* is associated with each of the plurality of target devices, as recited in independent claims 16 and 25.

The Leung reference also cannot be read as describing an initiator device is configured to multicast the transaction request to the plurality of target devices using a *single base address* associated with the plurality of target devices, wherein the same *single base address* is associated with each of the plurality of target devices, as recited in independent claims 16 and 25 because the Leung reference specifically describes its memory modules as equipped with independent address and command decoders so that they function as independent units, *each with their own base address*. *See* Leung, col. 3, lines 31-34.

As such, the Examiner has failed to show that the Leung reference and/or the Guttag reference, taken either alone or in hypothetical combination, teach all elements of independent claims 16 and 25. Therefore, Appellants respectfully request the Board reverse the Examiner's rejection under 35 U.S.C. § 103 of independent claims 16 and 25, as well as all claims depending therefrom.

F **Examiner's Argument Regarding Claims 17, 18, 26, and 27:**

Similar to claims 5 and 6 discussed above, claims 17, 18, 26, and 27 recite "the target devices comprise input/output controllers" and "the target devices comprise disk array

controllers." The Examiner again argued the non-limiting nature of the term "comprise." *See* Examiner's Answer, page 33. The Examiner must show that the prior art teachings *include* input/output controllers and disk array controllers to properly maintain a Section 103 rejection of claims 10 and 11. *See* M.P.E.P. 2111.03. The Leung reference, at best shows memory arrays that may be simultaneously written to, but does not show that these memory arrays comprise either input/output controllers and/or disk array controllers as recited in claims 17, 18, 26, and 27. Therefore, the applied prior art fails to teach all elements of claims 17, 18, 26, and 27. Accordingly, because the Examiner has failed to show all elements of claims 17, 18, 26, and 27 in the prior art, Appellants respectfully request the Board reverse the Examiner's rejection under 35 U.S.C. § 103 of claims 17, 18, 26, and 27.

G. **Examiner's Argument Regarding Claims 32:**

In the Examiner's Answer, with respect to independent claim 32, the Examiner argued that the Guttag reference failed to disclose a plurality of devices having a common base address wherein each of the devices simultaneously accesses its associated interleaved memory region in response to a single transaction request directed to the common base address. *See* Examiner's Answer, pages 13-14. To obviate this deficiency, the Examiner relied on the Gupta reference. Specifically, the Examiner stated that the Gupta reference teaches a plurality of devices having a common base address wherein each of the devices simultaneously accesses its associated interleaved memory region in response to a single transaction request directed to the common base address. *See* Examiner's Answer, page 14.

However, contrary to this assertion by the Examiner, the Gupta reference does not teach a plurality of devices having a common base address wherein each of the devices *simultaneously accesses* its associated interleaved memory region in response to a *single transaction request* directed to the *common* base address. Indeed, the Gupta reference explicitly teaches that separate memory busses are used to access the interleaved memory, and more importantly, that the separate memory busses *cannot receive the same type of operation at the same time. See* Gupta, col. 8, lines 35-40. Accordingly, because the separate memory busses of the Gupta reference cannot receive the same type of operation at the same time, the Gupta reference cannot be read as simultaneously accessing associated interleaved memory region in response to a *single transaction request* since a single transaction request would force the separate memory busses to receive the same type of operation at the same time. Instead, because the separate memory busses of the Gupta reference cannot receive the same type of operation at the same time, the Gupta reference teaches, at best, accessing *two memory region* with *two requests* simultaneously.

Moreover, contrary to the assertions of the Examiner (*see* Examiner's Answer, page 37) the Blaner reference cannot be applied to overcome the deficiencies of the Gupta reference because the Blaner reference describes, at best, accessing *one memory region* with *one request. See* Blaner, Fig. 1, ref. 116. Therefore, both the Blaner and Gupta references fail to teach *each of the plurality of devices* associated with one of the interleaved memory regions wherein each of the devices *simultaneously* accesses its associated interleaved memory region in response to a *single transaction request* directed to the common base address, i.e., simultaneously accessing at least *two memory regions* with a *single request*, as recited in independent claim 32.

As such, the Examiner has failed to show that the Guttag, the Gupta, and/or the Blaner references, taken either alone or in hypothetical combination, teach all elements of independent claim 32. Therefore, Appellants respectfully request the Board reverse the Examiner's rejection under 35 U.S.C. § 103 of independent claim 32, as well as all claims depending therefrom.

H. **Examiner's Argument Regarding Claims 33:**

In the Examiner's Answer, with respect to independent claim 33, the Examiner argued that the Guttag reference discloses a plurality of n processors with a corresponding plurality of memories, with the plurality of memories having a corresponding base address. *See* Examiner's Answer, page 38. As described above with respect to the rejection of independent claim 1, the Guttag reference describes a plurality of memories that, at best, correspond to *both* a parameter memory base address *and* a data memory base address, that is, *two* base addresses. *See* Guttag, col. 5, lines 63-66. Accordingly, the Guttag reference cannot be read as describing associating a plurality of target devices with a single base memory address, wherein the same single base memory address is associated with each of the plurality of target devices, and *executing a memory access using the single base memory address*, as recited in independent claim 33.

The Leung reference also cannot be read as describing *executing a memory access using the single base memory address*, as recited in independent claim 33 because the Leung reference specifically describes its memory modules as equipped with independent address and command decoders so that they function as independent units, *each with their own base address*. *See* Leung, col. 3, lines 31-34.

Furthermore, neither the Leung reference, the Guttag, nor the Gupta references describe associating the plurality of target devices with a *single base memory address*, wherein the *same single base memory address* is associated with each of the plurality of target devices, and executing a memory access using the single base memory address. Specifically, the Leung, Guttag, and Gupta references describe only the access of memory; they do not describe association of a first and a second target device, *separate from memory*, associated with the same single base address, as recited in independent claim 33. Accordingly, the Leung, Guttag, and Gupta references cannot be read as teaching associating the *plurality of target devices* with a *single base memory address*, wherein the *same single base memory* address is associated with *each of the plurality of target devices*.

As such, the Examiner has failed to show that the Leung reference, the Guttag reference and/or the Gupta reference, taken either alone or in hypothetical combination, teach all elements of independent claim 33. Therefore, Appellants respectfully request the Board reverse the Examiner's rejection under 35 U.S.C. § 103 of independent claim 33, as well as all claims depending therefrom.

I. Examiner's Argument Regarding Claims 36:

In the Examiner's Answer, with respect to independent claim 36, the Examiner argued that the Guttag reference discloses a plurality of n processors with a corresponding plurality of memories, with the plurality of memories having a corresponding base address. *See* Examiner's Answer, page 38. As described above with respect to the rejection of independent claim 1, the Guttag reference describes a plurality of memories that, at best, correspond to *both* a parameter

memory base address *and* a data memory base address, that is, *two* base addresses. *See* Guttag, col. 5, lines 63-66. Accordingly, the Guttag reference cannot be read as describing code to *associate the single base address* with a plurality of interleaved memory regions, wherein the *same single base address* is associated with each of the plurality of interleaved memory regions, as recited in independent claim 36.

The Leung reference also cannot be read as describing code to configure the plurality of devices to associate code to *associate the single base address* with a plurality of interleaved memory regions, wherein the *same single base address* is associated with each of the plurality of interleaved memory regions, as recited in independent claim 36, because the Leung reference specifically describes its memory modules as equipped with independent address and command decoders so that they function as independent units, *each with their own base address*. *See* Leung, col. 3, lines 31-34.

Furthermore, neither the Leung reference, the Guttag, nor the Gupta references describe code to configure the plurality of devices to associate a *single base address* with the plurality of *devices*, wherein the *same single base address* is associated with *each of the plurality of devices*, as recited in independent claim 36. Specifically, the Leung, Guttag, and Gupta references describe only the access of memory; they do not describe association of a first and a second target device, *separate from memory*, associated with the same single base address, as recited in independent claim 36. Accordingly, the Leung, Guttag, and Gupta references cannot be read as teaching code to configure the plurality of devices to associate a *single base address* with the

plurality of *devices*, wherein the *same single base address* is associated with *each of the plurality of devices*, as recited in independent claim 36.

As such, the Examiner has failed to show that the Leung reference, the Guttag reference and/or the Gupta reference, taken either alone or in hypothetical combination, teach all elements of independent claim 36. Therefore, Appellants respectfully request the Board reverse the Examiner's rejection under 35 U.S.C. § 103 of independent claim 36, as well as all claims depending therefrom.

J. **Examiner's Argument Regarding Claims 47:**

In the Examiner's Answer, with respect to independent claim 47, the Examiner argued that the Guttag and Gupta references failed to teach initiating an interleaved memory operation as a single request to the collective target group using the common base address, wherein each disk drive recognizes the common base address and simultaneously executes the memory operation on the portion of data storage to which the disk drive is assigned. *See* Examiner's Answer, page 16. To obviate this deficiency, the Examiner relied on the Blaner reference. *See id.*

However, contrary to the assertion by the Examiner, the Blaner reference does not teach initiating an interleaved memory operation as a *single request to the collective target group* using the common base address, wherein each disk drive recognizes the common base address and simultaneously executes the memory operation on the portion of data storage to which the disk drive is assigned. The Blaner reference describes, at best, accessing *one memory region* with *one*

request. *See* Blaner, Fig. 1, ref. 116. Furthermore, the Gupta reference explicitly teaches accessing two memory regions via separate memory busses whereby the separate memory busses *cannot receive the same type of operation at the same time*. *See* Gupta, col. 8, lines 35-40. Accordingly, because the separate memory busses of the Gupta reference cannot receive the same type of operation at the same time, the Gupta reference teaches, at best, accessing *two memory regions* with *two requests* simultaneously. Therefore, both the Blaner and Gupta references fail to teach initiating an interleaved memory operation as a *single request* to the *collective target group* using the *common base address*, i.e., simultaneously accessing at least *two memory regions* with a *single request*, as recited in independent claim 47.

As such, the Examiner has failed to show that the Guttag, the Gupta, and/or the Blaner references, taken either alone or in hypothetical combination, teach all elements of independent claim 47. Therefore, Appellants respectfully request the Board reverse the Examiner's rejection under 35 U.S.C. § 103 of independent claim 47, as well as all claims depending therefrom.

Conclusion

The foregoing are reiterative or supplemental points regarding the reasons why the pending claims are allowable. Appellants rely upon all of the reasons advanced in the Appeal Brief, and respectfully request that the Board carefully review the claims in view of these arguments and overturn the Examiner's rejection.

Respectfully submitted,

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